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PATENT APPLICATION
Docket No. 15436.330.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of	Gerald L. Dybsetter et al.	)
		)
Serial No.:	10/814,392	)
		)
Filed:	March 31, 2004	)
		)
Confirmation No.:	5366	) Art Unit
		) 2185
For:	CONTINGENT PROCESSOR TIME DIVISION MULTIPLE ACCESS OF MEMORY IN A MULTI-PROCESSOR SYSTEM TO ALLOW SUPPLEMENTAL MEMORY CONSUMER ACCESS	)
		)
Examiner:	Yaima Campos	)
		)
Appeal No.:	_____	)

The Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

REPLY BRIEF OF APPELLANTS PURSUANT TO 37 CFR 41.41

This Reply Brief is responsive to the Examiner's Answer mailed 11 March 2008 (the "Examiner's Answer") and is hereby submitted to the Board of Patent Appeals and Interferences (the "Board") pursuant to the provisions of 37 CFR 41.41.

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LIST OF REFERENCES

U.S. PATENT DOCUMENTS

U.S. Patent No. 6,401,176 to *Fadavi-Ardekani, et al.*
U.S. Patent No. 5,893,153 to *Tzeng, et al.*
U.S. Patent No. 6,275,885 to *Chin, et al.*
U.S. Patent No. 5,999,299 to *Chan, et al.*

I. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Issue 1: Whether claims 1-6 and 9-33 are unpatentable, under 35 U.S.C. §103(a), as being obvious over U.S. Patent No. 6,401,176 to Fadavi-Ardekani, et al. ("*Fadavi-Ardekani*") in view of U.S. Patent No. 5,893,153 to Tzeng, et al. ("*Tzeng*").

Issue 2: Whether claims 7 and 8 are unpatentable, under 35 U.S.C. §103(a), as being obvious over *Fadavi-Ardekani* and *Tzeng* as applied to claim 6, and further in view of U.S. Patent No. 6,275,885 to Chin, et al. ("Chin").

Issue 3: Whether claims 34 and 40-42 are unpatentable, under 35 U.S.C. §103(a), as being obvious over *Fadavi-Ardekani* and *Tzeng* as applied to claim 28, and further in view of assertions by the Examiner that it would have been obvious to use the memory controller as claimed in these claims.

Issue 4: Whether claims 35-39 are unpatentable, under 35 U.S.C. §103(a), as being obvious over *Fadavi-Ardekani* and *Tzeng* as applied to claim 34, and further in view of assertions by the Examiner that it would have been obvious to apply the memory controller as claimed in these claims to a laser transmitter/receiver of 1 G, 2 G, 4 G, 10 G, or greater than 10 G.

II. REPLY TO EXAMINER ARGUMENTS

Applicants note at the outset that the remarks, or a lack of remarks, herein are not intended to constitute, and should not be construed as, an acquiescence on the part of the Applicants: as to the purported teachings or prior art status of the cited references; as to the characterization of the cited references advanced by the Examiner; or as to any other assertions, allegations or characterizations made by the Examiner at any time in this case.

A. Executive Summary

The issues in this case appear to boil down to a fundamental misunderstanding on the part of the Examiner as to what each of the independent claims 1, 20, and 28 require, and as to what the primary reference, *Fadavi-Ardekani*, does or does not teach. Applicants will attempt in this Executive Summary to briefly frame these issues.

It may be helpful to discuss the claims in connection with the example embodiments disclosed in Figures 1 and 2 of the present application. It is understood that the claims are not limited to the example embodiments disclosed in Figures 1 and 2 (and specified below in parenthesis), and that these Figures are used here by way of illustration only and not by way of limitation.

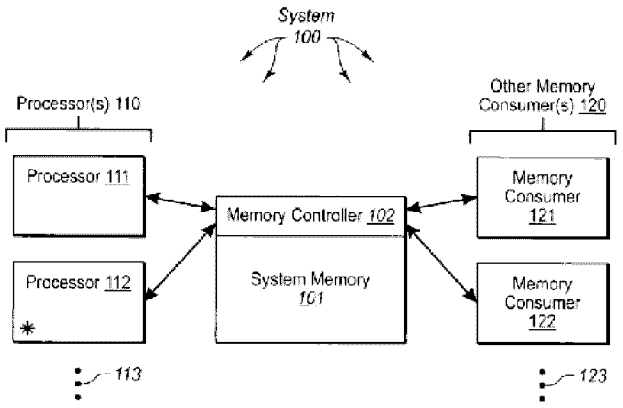


Fig. 1

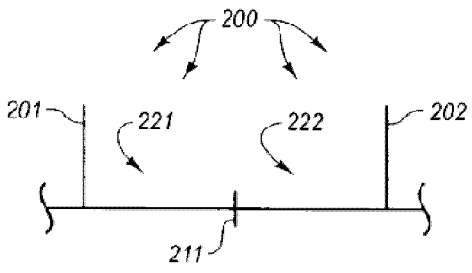


Fig. 2

With reference first to Figure 1, each of the rejected independent claims 1, 20, and 28 require, "a first processor" (111), "a second processor" (112), "one or more other memory consumers" (121), a "memory controller" (102), and a "system memory" (101). With reference now to Figures 1 and 2, the claims require that the "memory controller" (102) perform or be configured to perform:

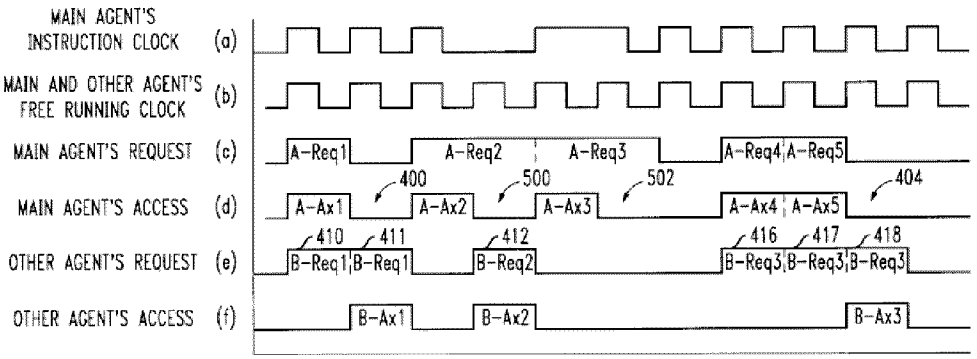
> an act of [] allotting a first division (221) … for a first processor (111) … such that memory access is guaranteed for the first processor (111) during the first division (221) … ; and
>
> an act of [] allotting a second division (222) …for a second processor (112) … such that memory access is conditionally granted to the second processor (112) during the second division (222) … *subject to* a determination that at least one of the one or more other memory consumers (121) has not also requested access to the system memory (101).

(Emphasis added). Thus, each of the rejected independent claims 1, 20, and 28 require that "a first division" (221) be allotted for a first processor (111), and "a second division" (222) be allotted for a second processor (112), with memory access during the first division (221) being "guaranteed" for the first processor (111), and memory access during the second division (222) being "conditionally granted" to the second processor (112) "*subject to* a determination that at least one of the one or more other memory consumers (121) has not also requested access to the system memory (101)." Therefore, claims 1, 20 and 28 require a fixed "second division" (222) of each memory access cycle (200) that is *specifically allotted for* the second processor (112), and that is *in fact "granted"* to the second processor (112) where it is determined that "one or more other memory consumers (121) has not also requested access to the system memory (101)," *without reference* to whether the first processor (111) has requested memory access during the "second division" (222) or not. That is, first and second "divisions" of each memory access cycle are thus *pre-allotted* for use by certain memory users, at least under certain conditions.

In contrast, each of the *Fadavi-Ardekani* systems appear to allow all memory access clock cycles to be dynamically allotted to memory users on a case-by-case basis and impose no restriction whatsoever on the ability of a "super agent" or a "main agent" (which the Examiner has characterized as the claimed "first processor") to request and obtain memory access "whenever requested" (for at least one memory access clock cycle, as discussed below). *See col 8, lines 54-57* ("With higher priority, the super agent is given access to the shared synchronous memory *whenever requested* and can thus access the shared synchronous memory *without halting its operation*."). In other words, *whenever* a "super agent" or "main agent" (the terms "super" and "main" appear to be used interchangeably in *Fadavi-Ardekani*) requests access to a memory access clock cycle, the memory access clock cycle is consistently granted to the main/super agent, without the system of *Fadavi-Ardekani* ever concerning itself whether the present memory access clock cycle is a pre-allotted "first division" or a "second division," nor whether "one or more other memory consumers has requested memory access during" a "second division" of each memory access cycle, as required by each of the rejected independent claims 1, 20, and 28.

This distinction between the rejected independent claims 1, 20, and 28 and the system of *Fadavi-Ardekani* is illustrated in Fig. 6:

FIG. 6



The system illustrated in Fig. 6 of *Fadavi-Ardekani* clearly grants access to any memory access clock cycle to the "main agent" *whenever* the "main agent" requests access to the memory access cycle. For example, each of the "main agent's" memory access requests (A-Req1, A-Req2, A-Req3, A-Req4, and A-Req5) are granted (A-Ax1, A-Ax2, A-Ax3, A-Ax4, and A-Ax5) despite simultaneous memory access requests by the "other agent" (see, e.g., the first B-Req1, the first B-Req1, and the second B-Req1). Notably, the system of Fig. 6 never appears to concern itself with determining whether the current memory access cycle is a pre-allotted "first division" or "second division," nor whether "one or more other memory consumers has requested memory access during" a second division of the current memory access cycle, as required by each of the rejected independent claims 1, 20, and 28.

Although the system of Fig. 6 of *Fadavi-Ardekani* does appear to allow memory access to an "other agent" where the "main agent's" requests access to multiple memory access clock cycles (see, e.g., A-Req2), it is noted that when the "main agent" and the "other agent" request access to the same memory access clock cycle, the "main agent" is always given priority and granted access (see, e.g., A-Req1, A-Req2, and A-Req3) despite simultaneous memory access requests by the "other agent" (see, e.g., the first B-Req1, the first B-Req1, and the second B-Req1) and without any attempt to determine whether the initial requested memory access clock cycles is a pre-allotted "first division" or "second division," nor whether "one or more other memory consumers has requested memory access during" a second division of the current memory access cycle, as required by each of the rejected independent claims 1, 20, and 28.

Thus, the system of Fig. 6 of *Fadavi-Ardekani* none the less appears to consider the allocation of each memory access cycle on a case-by-case basis, and appears to grant memory access to a "main agent" *whenever* the "main agent" *initially* requests access to memory without

being constrained by memory access requests by "other agents" nor by any pre-allotted memory access timeframes. In contrast with claims 1, 20, and 28, and considered in terms of *Fadavi-Ardekani* components, there appears to be no regular "second division" of each memory access cycle that is specifically "allotted" for the "other agent" to the exclusion of the "main agent." The systems of *Fadavi-Ardekani* therefore fail to satisfy the limitation of rejected independent claims 1, 20, and 28 that requires that a "second division" of each memory access cycle be *allotted* and *granted* to a "second processor…*subject to* a determination that at least one of the one or more other memory consumers has not also requested access to the system memory." No such "second division" that is specifically allotted for the second processor and the one or more other memory consumers appears to exist in the system of *Fadavi-Ardekani* because every single memory access clock cycle in the system of *Fadavi-Ardekani* appears to be available to the super/main agent (for at least one memory access cycle) so that the super/main agent of *Fadavi-Ardekani* can gain memory access "whenever requested" "without halting its operation."

Applicants will now address each of the Examiner's arguments in the order they appeared in the Examiner's Answer.

B. Issue 1: Whether claims 1-6 and 9-33 are unpatentable, under 35 U.S.C. §103(a), as being obvious over *Fadavi-Ardekani* in view of *Tzeng*.

i. The Examiner has failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claims 1-6 and 9-33

a. Claims 1, 20, and 28

In response to Applicants' argument that *Fadavi-Ardekani* does not teach that a non-super agent is allotted "a second division of each of the plurality of memory access cycles…such that memory access is conditionally granted to" the non-super agent "during the second division" as required by each of claims 1, 20, and 28, it appears that the Examiner has asserted that

Fadavi-Ardekani teaches an irrelevant condition that is different from the condition that is *actually recited* in claims 1, 20, and 28. In particular, the Examiner has asserted that:

> …processors and peripheral devices arbitrate/compete for memory access during a second memory access cycle, and access is granted to a processor on a conditional basis which comprises the *condition* that the super-agent is not accessing memory or has accessed memory for an extended time period."

Examiner's Answer, at 18. That is, it appears that the Examiner has asserted that *Fadavi-Ardekani* teaches that a non-super agent is "conditionally granted" access to memory subject to "the *condition* that the super-agent is not accessing memory or has accessed memory for an extended time period."

Notwithstanding the Examiner's assertion however, claims 1, 20, and 28 require that memory access be "conditionally granted" to the second processor "*subject to* a determination that at least one of the one or more other memory consumers has not also requested access to the system memory" and *not* subject to "the *condition* that the super-agent is not accessing memory or has accessed memory for an extended time period" as asserted by the Examiner. The rejected independent claims 1, 20, and 28 make *no* reference to the memory access that is "conditionally granted" to the second processor being dependent on the memory access of the first processor (i.e. a super-agent, according to the Examiner). Instead, the memory access that is "conditionally granted" to the second processor during the second division of each memory access cycle in claims 1, 20, and 28 is dependent *only* on "one or more *other* memory consumers [not having] also requested access to the system memory," *without reference to* whether the first processor has also requested access to memory.

The system of *Fadavi-Ardekani* provides "that the super agent A is provided *transparent access* to the shared synchronous memory 200, i.e., *whenever desired*." Col 5, lines 62-65. Further, "With higher priority, the super agent is given access to the shared synchronous memory

whenever requested and can thus access the shared synchronous memory *without halting its operation*." Col 8, lines 54-57.

In contrast to the system of *Fadavi-Ardekani*, the "first processor" of the methods of claims 1, 20, or 28 cannot access memory "whenever desired." For example, if the "first processor" were to request access to memory during "a second division of each of the plurality of memory access cycles," the request would be *denied* by the "memory controller" in the case where "one or more other memory consumers has not also requested access to the system memory," in which case a second processor would *instead* be granted memory access. Thus, the methods of claims 1, 20, and 28 do not guarantee memory access to the first processor "whenever desired" as taught by *Fadavi-Ardekani*, but instead guarantee access to the first processor only during a first division of each memory access cycle. During a second division of each memory access cycle, on the other hand, memory access is granted to a second processor as long as "one or more other memory consumers has not also requested access to the system memory."

In response to Applicants' argument that *Fadavi-Ardekani* teaches that a super agent can access memory "*whenever requested*," which necessarily includes "during the second division of each of [a] plurality of memory access cycles" as required by claims 1, 20, and 28, the Examiner has asserted that:

> First, the Examiner would like to respectfully point out that it appears that Appellant is misconstruing the rejection to the claims and has ignored the fact that a non-super agent or second processor accesses memory during open windows which not only exist when the super-agent or first processor is not accessing memory, but also when the super-agent has extended access lasting more than a single memory clock cycle/first division of a plurality of memory access cycles [Refer to Fadavi-Ardekani (Col. 6, lines 20-39 and 44-49; Col. 8, lines 20-24)]; therefore, as Fadavi-Ardekani discloses granting access to a non-super agent during an open-window, it is disclosed conditionally granting access

to a second processor or non-super agent during a second division of a plurality of memory access cycles.

Examiner's Answer, at 18-19. As to the Examiner's assertion that "as Fadavi-Ardekani discloses granting access to a non-super agent during an open-window, it is disclosed conditionally granting access to a second processor or non-super agent during a second division of a plurality of memory access cycles," it appears that the Examiner has again ignored the condition that is *actually recited* in claims 1, 20, and 28. As noted above, claims 1, 20, and 28 require that memory access be "conditionally granted" to the second processor "*subject to* a determination that at least one of the one or more other memory consumers has not also requested access to the system memory." Despite the Examiner's assertion regarding the "open-window" disclosed in *Fadavi-Ardekani*, the Examiner has failed to demonstrate that memory is grated to the second processor only after being "*subject to* a determination that at least one of the one or more other memory consumers has not also requested access to the system memory" as required by claims 1, 20, and 28.

Further, the fact remains that the super-agent of *Fadavi-Ardekani* can gain memory access "whenever requested" (for at least one memory access cycle) "without halting its operation." Therefore, even if *Fadavi-Ardekani* teaches an embodiment in Fig. 6 where cycles subsequent to a first requested cycle granted to a super-agent are opened up as windows for a non-super agent, this embodiment of Fig. 6 does not anticipate the method of claims 1, 20, and 28 because Fig. 6 fails to disclose a fixed "second division" of each memory access cycle that is *specifically "allotted" for* the second processor and the one or more other memory consumers, *regardless* of whether the first processor has requested memory access during the second division. Instead, the Examiner has not shown any restriction whatsoever in *Fadavi-Ardekani* on the ability of the super-agent to request and obtain memory access "whenever requested" (for at

least one memory access cycle). The system of *Fadavi-Ardekani* thereby fails to satisfy the limitation of claims 1, 20, and 28 that requires that a "second division" of each memory access cycle be *allotted* and *granted* to a "second processor…*subject to* a determination that at least one of the one or more other memory consumers has not also requested access to the system memory." No such "second division" that is specifically allotted for the second processor and the one or more other memory consumers appears to exist in the system of *Fadavi-Ardekani* because every single memory access cycle in the system of *Fadavi-Ardekani* appears to be available to the super agent so that the super-agent of *Fadavi-Ardekani* can gain memory access "whenever requested" "without halting its operation."

The Examiner has also asserted that:

> Appellant should note that the claims require conditionally granting memory access to a second processor or non-super agent during the second division of a plurality of memory access cycles; therefore, when memory is granted to a non-super agent during an open window…memory is conditionally granted to a non-super agent during a second division of a plurality of memory access cycles under the condition that a super-agent is not accessing memory or has accessed memory for more than one cycle.

Examiner's Answer, at 19 (emphasis in original). It appears that the Examiner has once again asserted that *Fadavi-Ardekani* teaches an irrelevant condition that is *different from* the condition that is actually recited in claims 1, 20, and 28. In particular, the Examiner has identified "the condition that a super-agent is not accessing memory or has accessed memory for more than one cycle." However, as discussed above, the rejected independent claims 1, 20, and 28 make *no* reference to the memory access that is "conditionally granted" to the second processor being dependent on the memory access of the first processor (i.e. a super-agent, according to the Examiner). Instead, the memory access that is "conditionally granted" to the second processor in claims 1, 20, and 28 is recited in the claims as being dependent *only* on "one or more *other*

memory consumers [not having] also requested access to the system memory," *without making reference to* whether the first processor has also requested access to memory.

The Examiner has further asserted that:

> Furthermore, even as Fadavi-Ardekani discloses super agent can access memory whenever requested; there is no requirement in the claims preventing super-agent from doing so, since the claims expressly require that access to a non-super agent or second processor be granted conditionally; therefore, it is irrelevant whether the first processor is able to take over a memory access that was granted to a second processor or non-super agent during a second division of a plurality of memory access cycles, since this access was only conditionally granted to the non-super agent or second processor, as required by the claims.

Examiner's Answer, at 19 (emphasis in original).

In response to the Examiner's assertion above that "there is no requirement in the claims preventing super-agent from [accessing memory whenever requested]," Applicants note that the ability of the super-agent of *Fadavi-Ardekani* to access memory "whenever requested" would *prevent* the second processor from being "granted" memory access, as *required* by claims 1, 20, and 28, during the "second division" of a memory access cycle if "at least one of the one or more other memory consumers has not also requested access to the system memory."

In response to the Examiner's assertion above that "it is irrelevant whether the first processor is able to take over a memory access that was granted to a second processor or non-super agent during a second division of a plurality of memory access cycles, since this access was only conditionally granted to the non-super agent or second processor, as required by the claims," Applicants note that the methods of claims 1, 20, and 28 do not include elements dealing with the *first* processor having the "ab[ility] to take over a memory access that was granted to a *second* processor" as asserted by the Examiner. *Rather*, the methods of claims 1, 20, and 28, require the guaranteeing of a first division of each of a plurality of memory access cycles to a *first* processor, and the granting of a second division of each of the plurality of memory

access cycles to a *second* processor *conditioned only on* "a determination that at least one of the one or more *other* memory consumers has not also requested access to the system memory." (Emphasis added). Claims 1, 20, and 28 clearly require that if the condition recited in these claims is satisfied, the second processor is "granted" access to memory by the memory controller.

Thus, the unconditional access to memory of the super-agent of *Fadavi-Ardekani* "*whenever* requested" (which presumably includes during any "second division" of a memory access cycle) is simply inconsistent with the requirements of claims 1, 20, and 28 that the *second* processor be granted access upon a determination that the "one or more other memory consumers has not also requested access to the system memory."

The preceding statement by the Examiner also appears to misconstrue the meaning of the phrase "conditionally granted." In response, Applicants note the following statement from the specification:

> ...The memory controller 102 only conditionally grants memory access to the second processor during the second division subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory. A processor that has such conditional access during its time division in the memory access cycle will also be referred to herein as a "conditioned processor".

Specification, at [0028]; *see also Specification*, at [0031] and Figure 5. It is clear from the plain language of the claims, and consistent with the specification, that the term "conditionally" in the phrase "conditionally granted" of claims 1, 20, and 28 refers to a determination as to whether memory access *should be granted* by the memory controller and, contrary to assertions of the Examiner, does *not* refer to a determination as to whether memory access *should be retained once granted* by the memory controller.

In response to Applicants' argument that *Fadavi-Ardekani* teaches away from having an allotted "second division of each of a plurality of memory access cycles" for a second processor or other memory consumer(s) as required by claims 1, 20, and 28, because such an allotted portion would prevent the super agent from gaining memory access "whenever requested," the Examiner has asserted that:

> Fadavi-Ardekani clearly teaches [that] ... memory is conditionally granted to a non-super agent during a second division of a plurality of memory access cycles under the condition that a super-agent is not accessing memory or has accessed memory for more than one cycle. Furthermore, even as Fadavi-Ardekani discloses super agent can access memory whenever requested; there is no requirement in the claims preventing super-agent from doing so, since the claims expressly require that access to a non-super agent or second processor be granted conditionally; therefore, it is irrelevant whether the first processor is able to take over a memory access that was granted to a second processor or non-super agent during a second division of a plurality of memory access cycles, since this access was only conditionally granted to the non-super agent or second processor, as required by the claims.

Examiner's Answer, at 20-21. These assertions by the Examiner are deficient at least because the Examiner has once again asserted that *Fadavi-Ardekani* teaches an irrelevant condition that is *different from* the condition that is actually recited in claims 1, 20, and 28, and because the ability of the super-agent of *Fadavi-Ardekani* to access memory "*whenever* requested" would *prevent* the claimed second processor from being "granted" memory access during the "second division" of a memory access cycle if "at least one of the one or more other memory consumers has not also requested access to the system memory" as required by claims 1, 20, and 28, as discussed above.

The Examiner has further asserted that:

> Furthermore, the Examiner would also like to point out that the reference to Fadavi-Ardekani does not teach away from the claimed invention as Fadavi-Ardekani's disclosure does not criticize, discredit, or otherwise discourage the solution claimed *In re Fulton*, 391 F.3d 1195,1201,73 USPQ2d 1141, 1146 (Fed. Cir. 2004). See also MPEP 2123.

Examiner's Answer, at 21. In response to this assertion, Applicants note that the Examiner appears to have misconstrued the teaching of *In re Fulton* and MPEP 2123. The entire quote from *In re Fulton* in MPEP 2123(II) states "[t]he prior art's mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed..." (Emphasis added). As stated in MPEP 2141.02(VI), "A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention." (Emphasis in original) (citation omitted). In this case, the portions of *Fadavi-Ardekani* that teach that the super-agent can access the memory "whenever requested" so that the super-agent can access memory "without halting its operation" *lead away* from the invention of claims 1, 20, and 28 because these claims require that a "second division" of each memory access cycles be "granted" to a "second processor" if "at least one of the one or more other memory consumers has not also requested access to the system memory". *Compare, e.g.,* column 8, lines 54-57 ("...the super agent is given access to the shared synchronous memory *whenever requested* and can thus access the shared synchronous memory *without halting its operation*.").

b. Claims 16, 17, 24, 25, 32, and 33

In the interest of brevity, Applicants note that rejection of claims 16, 17, 24, 25, 32, and 33 are problematic for at least the same reasons set forth in the discussion of claims 1, 20, and 28 at II.A.i.a. above, and Applicants respectfully direct the attention of the Board to that discussion.

ii. The Examiner has failed to establish that there is a reasonable expectation of success in implementing the purportedly obvious combination of *Fadavi-Ardekani* and *Tzeng*

a. Claims 6, 9-14, 18, 19, 21-23, 26, 27, and 29-31

In the interest of brevity, Applicants simply note disagreement with the Examiner's conclusory statements that: "the Examiner…would like to point that the combination of Fadavi-Ardekani and Tzeng discloses all the limitations required by the claims as explained above," *Examiner's Answer*, at 25, and "In this case, both Fadavi-Ardekani and Tzeng…disclose all the limitations required by the claims," *Examiner's Answer*, at 26.

C. Issue 2: Whether claims 7 and 8 are unpatentable, under 35 U.S.C. §103(a), as being obvious over *Fadavi-Ardekani* and *Tzeng* as applied to claim 6, and further in view of U.S. Patent No. 6,275,885 to Chin et al. ("*Chin*").

i. The Examiner has failed to establish that there is a reasonable expectation of success in implementing the purportedly obvious combination of *Fadavi-Ardekani*, *Tzeng*, and *Chin*

In the interest of brevity, Applicants simply note disagreement with the Examiner's conclusory statements that: "the Examiner…would like to point that the combination of Fadavi-Ardekani, Tzeng, and Chin discloses all the limitations required by the claims as explained above," *Examiner's Answer*, at 26, and "In this case, Fadavi-Ardekani, Tzeng, and Chin…disclose all the limitation required by the claims," *Examiner's Answer*, at 27.

D. Issue 3: Whether claims 34 and 40-42 are unpatentable, under 35 U.S.C. §103(a), as being obvious over *Fadavi-Ardekani* and *Tzeng* as applied to claim 28, and further in view of assertions by the Examiner that it would have been obvious to use the controller as claimed in these claims.

i. The Examiner has failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claims 34 and 40-42

As noted in the Brief of Appellant, the rejected dependent claim 34 requires that a "memory controller *is implemented in* a laser transmitter/receiver." (Emphasis added). The rejected dependent claim 40 requires that "the laser transmitter/receiver *is* an XFP laser transceiver." The rejected dependent claim 41 requires that "the laser transmitter/receiver *is* an

SFP laser transceiver." The rejected dependent claim 42 requires that "the laser transmitter/receiver *is* a SFF laser transceiver."

In the *Examiner's Answer*, the Examiner included for the first time a reference to "Figure 4 and related text" of U.S. Patent No. 5,999,299 to Chan et al. ("*Chan*") "used as evidentiary reference" to support the Examiner's assertion that "it is well known in the art that a laser transceiver comprises a memory and a controller." *Examiner's Answer*, at 14.

Despite the assertion of the Examiner, Applicants note that it is the burden of the Examiner to clearly articulate the reason(s) why the claimed invention would have been obvious to one of ordinary skill in the art at the time the invention was made. *See* MPEP § 2141(III). As stated by the U.S. Supreme Court in *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. _____, 82 USPQ2d 1385 (2007), the analysis supporting a rejection made under 35 U.S.C. § 103 should be made explicit. Moreover, the Court also stated in *KSR* that "…[R]ejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Id.* at 1396.

Applicants note that the Examiner has made no effort in the Examiner's Answer to make "some articulated reasoning with some rational underpinning" why it would have allegedly been obvious to "implement" the "memory controller" of claim 34 in the "laser communication device" of *Chan*. Instead, the Examiner has attempted to sustain the rejection of claim 34 "by mere conclusory statements," which attempt is directly contrary to the requirements of *KSR*.

In response to Applicants' argument that the phrase "is implemented in" in claim 34 is not a statement of how the controller is intended to be used but instead requires a laser transmitter/receiver as a limitation of claim 34 in which the memory controller "*is* implemented," the Examiner has asserted that, "…claims 34 and 40-42 refer to some of the many possible

environments where applicant's invention *could be implemented* or used…" *Examiner's Answer*, at 27 (emphasis added). Despite the Examiner's assertion, Applicants note that claim 34 requires that the "memory controller *is* implemented in a laser transmitter/receiver," *not* that the memory controller "*could be* implemented in" in a laser transmitter/receiver as asserted by the Examiner. Therefore, claim 34, and claims 40-42 which each depend therefrom, require "a laser transmitter/receiver" as an express claim element.

E. Issue 4: Whether claims 35-39 are unpatentable, under 35 U.S.C. §103(a), as being obvious over *Fadavi-Ardekani* and *Tzeng* as applied to claim 34, and further in view of assertions by the Examiner that it would have been obvious to apply the memory controller as claimed in these claims to a laser transmitter/receiver of 1 G, 2 G, 4 G, 10 G, or greater than 10 G.

i. The Examiner has failed to establish that the cited references, when combined, teach or suggest all the limitations of rejected claims 35-39

As noted in the Brief of Appellant, rejected dependent claims 35-39 require that a "laser transmitter/receiver is "a 1G laser transceiver," "a 2G laser transceiver," "a 4G laser transceiver," "a 10G laser transceiver," or "a laser transceiver suitable for fiber channels greater than 10G," respectively.

In the *Examiner's Answer*, the Examiner included for the first time a reference to "Col. 1, lines 60-67" of U.S. Patent No. 5,999,299 to Chan et al. ("*Chan*") "used as evidentiary reference" to support the Examiner's assertion that "rendering different transfer rates/bandwidths of transceiver as a characteristic of a laser transceiver that is well known in the art." *Examiner's Answer*, at 29.

Despite the assertion of the Examiner, Applicants note that the Examiner has made no effort in the *Examiner's Answer* to make "some articulated reasoning with some rational underpinning" why it would have allegedly been obvious to "implement" the "laser communication device" of *Chan* as "a 1G laser transceiver," "a 2G laser transceiver," "a 4G

laser transceiver," "a 10G laser transceiver," or "a laser transceiver suitable for fiber channels greater than 10G," as required by claims 35-39, respectively. Instead, the Examiner has attempted to sustain the rejection of claim 34 "by mere conclusory statements," which attempt is directly contrary to the requirements of *KSR* noted above.

In response to Applicants' argument that *Fadavi-Ardekani* and *Tzeng* do not disclose a laser transmitter/receiver that is "a 1G laser transceiver," "a 2G laser transceiver," "a 4G laser transceiver," "a 10G laser transceiver," or "a laser transceiver suitable for fiber channels greater than 10G," as required by claims 35-39, respectively, the Examiner has asserted that, "...claims 35-39 refer to different characteristics of some of the many possible environments where applicant's invention *could be implemented* or used..." *Examiner's Answer*, at 28 (emphasis added). Despite the Examiner's assertion, Applicants note that claim 34, from which claims 35-39 each depend, requires that the "memory controller *is* implemented in a laser transmitter/receiver," *not* that the memory controller "*could be* implemented in" in a laser transmitter/receiver as asserted by the Examiner. Therefore, claim 34, and claims 35-39 which each depend therefrom, require "a laser transmitter/receiver" as an express claim limitation.

The Examiner has also asserted,

> Furthermore, claims 35-39 involve a mere change in bandwidth size of the transmitter/receiver claimed in claim 34. Applicant should note that such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955)."

Examiner's Answer, at 29.

Applicants respectfully submit that while the Examiner has relied on *In re Rose* as supporting the rejection under 35 USC 103, the Examiner has failed to demonstrate any similarity between the facts of *In re Rose* and the facts in the present case. As the examination

guidelines make clear "…legal precedent can provide the rationale supporting obviousness only if the facts in the [cited] case are similar to those in the application." *MPEP § 2144. Emphasis added.* Inasmuch as the Examiner has failed to assert, much less establish, that the facts in the cited case are similar to those in the application, the rejection lacks an adequate foundation and should accordingly be withdrawn.

In addition, Applicants note the Examiner has failed to demonstrate that the "1G," "2G," "4G," "10G," or "greater than 10G," elements of claims 35-39 relate to "the *size* of a component" as alleged by the Examiner. On the contrary, Applicants note that these claim elements clearly refer to the *data rate* of a transceiver, not necessarily to the *size* of a transceiver. Therefore, the Examiner's reliance on *In re Rose* in the rejection of claims 35-39 is not well taken as *In re Rose* makes no mention of the *data rate* of a transceiver.

CONCLUSIONS

Based on the foregoing, Appellants respectfully submit that the rejections of the claims are not well taken. Accordingly, Appellants respectfully request that the Board reverse the Examiner's rejections of claims 1-42 pending in this application and thereby place this application in condition for immediate allowance.

DATED this the 12th day of May, 2008.

Respectfully submitted,

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